IN THE CLAIMS:

1. (Previously presented) A semiconductor integrated circuit device, comprising:

a semiconductor substrate; and

memory cell MISFETs formed on a principal plane of the semiconductor substrate and provided with gate electrodes that are coupled to word lines extending in a first direction of the principal plane, wiring grooves formed in a first insulating film over the memory cell MISFETs, the wiring grooves extending in a second direction intersecting the first direction and having a second insulating film formed on side walls thereof, bit lines formed inside the wiring grooves and electrically connected to one of sources and drains of the memory cell MISFETs, and data storing capacitors formed over the bit lines and electrically connected to the other one of the sources and drains,

wherein the bit lines are comprised of a first conductive film, and a second conductive film that has a higher adhesive strength to the second insulating film than the first conductive film and is formed on a boundary face between the second insulating film inside the wiring grooves and the first conductive film, and

wherein each of the wiring grooves extends in the second direction over the memory cells.

2. (Previously presented) A semiconductor integrated circuit device according to Claim 1, wherein the second conductive film is comprised of TiN.

3. (Previously presented) A semiconductor integrated circuit device according to Claim 1, wherein the second conductive film is comprised of TaN, WN, or ZrN.

4. (Previously presented) A semiconductor integrated circuit device according to Claim 1, wherein an inside width of the second insulating film formed on the wiring grooves is less than a minimum processing dimension that is determined by a resolution limit of a photolithography.

5. (Previously presented) A semiconductor integrated circuit device according to Claim 1, wherein the second insulating film contains a silicon oxide as the principal component.

6. (Previously presented) A semiconductor integrated circuit device according to Claim 1, wherein widths of the bit lines are narrower than a spacing between adjoining bit lines.

7. (Previously presented) A semiconductor integrated circuit device according to Claim 1, wherein the bit lines are electrically connected to one of the sources and the drains by way of plugs embedded inside first connection holes that are formed in a third insulating film underlying the first insulating film.

8. (Previously presented) A semiconductor integrated circuit device according to Claim 7, wherein the first connection holes have a larger diameter in the first direction than the diameter in the second direction, a part of the first connection holes extends on active regions where the memory cell selecting MISFETs are formed, and the other part of the holes extends on device isolation regions right beneath the bit lines.

9. (Previously presented) A semiconductor integrated circuit device according to Claim 1, wherein surfaces of the bit lines are equal in height to the surface of the first insulating film.

10. (Previously presented) A semiconductor integrated circuit device according to Claim 7, wherein each of the plugs is separately formed in each of the memory cells.

11. (Previously presented) A semiconductor integrated circuit device according to Claim 1, wherein the memory cell MISFETs are included in DRAM memory cells.

12. (Previously presented) A semiconductor integrated circuit device, comprising:

a semiconductor substrate; and

memory cell MISFETs formed on a principal plane of the semiconductor substrate and provided with gate electrodes that are coupled to word lines extending in a first direction of the principal plane, wiring grooves being formed in a first insulating film over the memory cell MISFETs, the wiring grooves extending in a second direction intersecting the first direction and having a second insulating film formed on side walls

thereof, bit lines being formed inside the wiring grooves and electrically connected to one of sources and drains of the memory cell MISFETs, and data storing capacitors formed over the bit lines and electrically connected to the other one of the sources and drains,

wherein the bit lines are comprised of a first conductive film, and a second conductive film that has a higher adhesive strength to the second insulating film than the first conductive film and is formed on a boundary face between the second insulating film inside the wiring grooves and the first conductive film, and

wherein each of the wiring grooves extends in the second direction over the memory cells.

13. (Withdrawn) A method of producing a semiconductor integrated circuit device comprising the steps of:

(a) forming a first insulating film having first grooves over a principal surface of a semiconductor substrate;

(b) forming conductive plugs in said first grooves of said first insulating film;

(c) forming a second insulating film having second grooves on said first insulating film;

(d) depositing a third insulating film having a film thickness that does not completely bury inside surfaces of said second grooves, on said second insulating film including said inside surfaces of said second grooves;

(e) forming sidewall spacers comprised of said third insulating film on said second grooves by applying an anisotropic etching to said third insulating film;

(f) depositing a first conductive film in said second grooves on said sidewall spacers and on said conductive plugs;

(g) depositing a second conductive film on said first conductive film;

(h) forming first wirings comprised of said first conductive film and said second conductive film on said inside surfaces of said second grooves, by polishing said second and first conductive films chemically and mechanically to remove said first and second conductive films that lie outside said second grooves,

wherein said first conductive film has a higher adhesive strength to said third insulating film than said second conductive film.

14. (Withdrawn) A method of producing a semiconductor integrated circuit device according to claim 13, wherein said first conductive film is comprised of TiN.

15. (Withdrawn) A method of producing a semiconductor integrated circuit device according to claim 13, wherein said first conductive film is one selected from the group comprising TaN, WN and ZrN.

16. (Withdrawn) A method of producing a semiconductor integrated circuit device according to claim 13, wherein at least one of the first wirings is a bit line of a DRAM.

17. (Withdrawn) A method of producing a semiconductor integrated circuit device according to claim 16, wherein the DRAM includes at least one MISFET with a data storing capacitor overlying the bit line.